Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method in a data processing system for processing instructions, the method comprising:

responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether [[an]] a performance indicator that identifies that execution of the instruction is to be monitored is present ~~associated with the instruction~~; and

forcing an interrupt if the performance indicator is present ~~associated with the instruction~~.

2. (Original) The method of claim 1, wherein the forcing step comprises:

sending a signal from an instruction cache to an interrupt unit in the processor; and

processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit.

3. (Original) The method of claim 2, wherein the processing step includes:

executing code associated with the interrupt.

4. (Original) The method of claim 3, wherein the code records cache misses by a functional unit attempting to access instructions in a cache.

5. (Currently amended) The method of claim 1, wherein the performance indicator is located in a shadow memory.

6. (Currently amended) The method of claim 1, wherein the instruction is received in a bundle and wherein the performance indicator comprises at least one [[spare]] bit in a field in the bundle.

7. (Currently amended) The method of claim 1, wherein the performance indicator is located in a field in the instruction.

8. (Currently amended) A method in a data processing system for processing data, the method comprising:

responsive to an access of data, determining whether [[an]] a performance indicator that identifies that access of the data is to be monitored ~~is associated with the data~~ is present; and

generating an interrupt if the ~~data is associated with the~~ performance indicator is present.

9. (Original) The method of claim 8, wherein the generating step comprises:

generating a signal by a data cache in which the data is located; and

receiving the signal generated by the data cache at an interrupt unit, wherein the signal indicates a presence of the interrupt to the interrupt unit.

10. (Original) The method of claim 8 further comprising:

processing the interrupt in an interrupt unit in response to generation of the interrupt.

11. (Original) The method of claim 10, wherein the processing step comprises:

executing a code for handling the interrupt.

12. (Currently amended) The method of claim 8, wherein the performance indicator identifies that access of the data is to be monitored ~~is associated with the data~~ through a specific value in a memory location for the data.

13. (Original) The method of claim 8, wherein the data is located in a memory location.

14. (Currently amended) A data processing system for processing instructions, the data processing system comprising:

determining means, responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, for determining whether [[an]] a performance indicator that identifies that execution of the instruction is to be monitored is present ~~associated with the instruction~~; and

forcing means for forcing an interrupt if the performance indicator is present ~~associated with the instruction~~.

15. (Original) The data processing system of claim 14, wherein the forcing means comprises:

sending means for sending a signal from an instruction cache to an interrupt unit in the processor; and

processing means for processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit.

16. (Original) The data processing system of claim 15, wherein the processing means includes:

executing means for executing code associated with the interrupt.

17. (Original) The data processing system of claim 16, wherein the code records cache misses by a functional unit attempting to access instructions in a cache.

18. (Currently amended) A data processing system for processing data, the data processing system comprising:

determining means, responsive to an access of data, for determining whether [[an]] a performance indicator ~~is associated with the data~~ that identifies that access of the data is to be monitored is present; and

generating means for generating an interrupt if ~~the data is associated with~~ the performance indicator is present.

19. (Original) The data processing system of claim 18, wherein the generating means comprises:

generating means for generating a signal by a data cache in which the data is located; and

receiving means for receiving the signal generated by the data cache at an interrupt unit, wherein the signal indicates a presence of the interrupt to the interrupt unit.

20. (Original) The data processing system of claim 18 further comprising:

processing means for processing the interrupt in an interrupt unit in response to generation of the interrupt.

21. (Currently amended) A computer program product in a computer readable medium for processing instructions, the computer program product comprising:

first instructions for responding to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether [[an]] a performance indicator that

identifies that execution of the instruction is to be monitored is present ~~associated with the instruction~~; and

second instructions for forcing an interrupt if the performance indicator is present ~~associated with the instruction~~.

22. (Currently amended) The computer program product of claim 21, wherein the second instructions include ~~forcing step comprises~~:

third instructions for sending a signal from an instruction cache to an interrupt unit in the processor; and

fourth instructions for processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit.

23. (Currently amended) The computer program product of claim 22, wherein the fourth instructions ~~includes~~ include;

sub-instructions for executing code associated with the interrupt.

24. (Currently amended) A computer program product in a computer readable medium for processing data, the computer program product comprising:

first instructions for responding to an access of data, determining whether [[an]] a performance indicator that identifies that access of the data is to be monitored is present ~~associated with the data~~; and

second instructions for generating an interrupt if ~~the data is associated with~~ the performance indicator is present.

25. (Currently amended) The computer program product of claim 24, wherein the second instructions comprise ~~comprises~~:

first sub-instructions for generating a signal by a data cache in which the data is located; and

second sub-instructions for receiving the signal generated by the data cache at an interrupt unit, wherein the signal indicates a presence of the interrupt to the interrupt unit.